

<b>Notice of References Cited</b>	Application/Control No. 09/648,540	Applicant(s)/Patent Under Reexamination SCHAPIRA ET AL.	
	Examiner Carlos Ortiz-Rodriguez	Art Unit 2125	Page 1 of 2

**U.S. PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-6,090,149	07-2000	Nair et al.	703/14
*	B US-6,100,830	08-2000	Dedic, Ian Juso	341/136
	C US-			
	D US-			
	E US-			
	F US-			
	G US-			
	H US-			
	I US-			
	J US-			
	K US-			
	L US-			
	M US-			

**FOREIGN PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

**NON-PATENT DOCUMENTS**

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
U	Thelen et al., "Simulating Mixed Analog-Digital Circuits on a Digital Simulator", IEEE, 1988.			
V	IEE Proceedings, Vol. 136, PT. G, No. 3, June 1989			
W	Shi et al., "Use of VHDL to Model and Simulate Analog-Digital IC's", IEEE, 1992.			
X	Minoura et al., "Structural Active Object Systems for Simulation", ACM, 1993.			

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<b>Notice of References Cited</b>	Application/Control No. 09/648,540	Applicant(s)/Patent Under Reexamination SCHAPIRA ET AL.	
	Examiner Carlos Ortiz-Rodriguez	Art Unit 2125	Page 2 of 2

**U.S. PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A US-			
	B US-			
	C US-			
	D US-			
	E US-			
	F US-			
	G US-			
	H US-			
	I US-			
	J US-			
	K US-			
	L US-			
	M US-			

**FOREIGN PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N				
	O				
	P				
	Q				
	R				
	S				
	T				

**NON-PATENT DOCUMENTS**

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
U	Chamberlain, "Parallel Logic Simulation of VLSI Systems", ACM, 1995.			
V	Low et al., "Cadence-based simulation of floating-gate circuits using the EKV model", IEEE, 1999.			
W	Yuan et al., "Floating-point analog-to-digital converter", IEEE, 1999.			
X				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.